WHAT IS CLAIMED IS:

1. A DRAM cell comprising:

A semiconductor substrate comprising an active region,

a word line driven by a row address;

a bit line driven by a column address;

a cell transistor having a source connected to the bit line and a gate electrode connected to the word line; and

a MOS capacitor comprising a storage node electrode connected to a drain of the cell transistor, a plate node electrode formed on the active region of the semiconductor substrate and an insulator thin film formed between the storage node electrode and the plate node electrode.

2. The DRAM cell of claim 1, wherein the storage node electrode has a T-shaped structure through a trench of the active region.

3. The DRAM cell of claim 1, further comprising a power line supplying a power voltage to the plate node electrode.

4. A DRAM cell comprising:

a semiconductor substrate comprising an active region;

a MOS capacitor comprising a plate node electrode disposed in the active region, a storage node electrode having a T-shaped structure through a trench of the active region and an insulator thin film formed between the plate node electrode and the storage node electrode;

a cell transistor comprising a gate insulating film and a gate electrode disposed on the top surface of the active region and a source/drain disposed in the active region;

an interlayer insulating film deposited on the MOS capacitor and the cell transistor;

a contact electrode connected to either the source/drain of the cell transistor or to the storage node electrode of the MOS capacitor through a contact hole in the interlayer insulating film;

a wire connected to the drain and the storage node electrode by the contact electrode; and

a bit line connected with the source by the contact electrode.

5. The DRAM cell of claim 4, wherein the MOS capacitor further includes a gap-fill layer filling a lower part of the trench with an insulating material.

6. The DRAM cell of claim 4, further comprising a power line for supplying a power voltage to the plate node electrode via an additional contact electrode of the interlayer insulating film.

7. The DRAM cell of claim 4, wherein the trench of the MOS capacitor is composed of curved trenches joined together by at least one linking trench.

8. The DRAM cell of claim 4, wherein a side wall spacer is disposed on side walls of the storage node electrode of the MOS capacitor and on side walls of the gate electrode of the cell transistor.

9. A method for manufacturing a DRAM cell, the method comprising:

forming a trench in an active region of a semiconductor substrate;

implanting impurities into the active region;

forming an insulator thin film and a gate insulating film simultaneously on the substrate and the trench;

forming a storage node electrode of a MOS capacitor having a T-shaped structure and a gate electrode of a cell transistor simultaneously by depositing a conductive film on the insulator thin film and the trench to bury the trench and then patterning the conductive film;

forming a source/drain of the cell transistor by implanting impurities into the resulting material;

forming a contact electrode connected to the source/drain of the cell transistor or to the storage node electrode of the MOS capacitor by forming an interlayer insulating film on the whole surface of the resulting material, forming a contact hole on the interlayer insulating film and then burying the conductive film into the contact hole; and

forming a wire connected with the drain and the storage node electrode and a bit line connected with the source through the contact electrode by depositing a conductive film on top of the interlayer insulating film and patterning the same.

10. The method of claim 9, wherein the trench of the MOS capacitor comprises a plurality of curved trenches joined together by at least one linking trench.

11. The method of claim 9, wherein a gap-fill layer is further formed for filling the lower part of the trench with an insulating material before implanting impurities into the active region.

12. The method of claim 11, wherein the gap-fill layer is formed on the trench of the storage node region of the MOS capacitor or on the trench of the device isolation region of the semiconductor substrate.

13. The method of claim 12, wherein the gap-fill layer formed on the trench of the storage node region of the MOS capacitor is buried down to a top surface of the trench or a predetermined portion thereof.

14. The method of claim 9, wherein a side wall spacer is additionally formed on the side walls of the storage node electrode of the MOS capacitor and on the side walls of the gate electrode of the cell transistor before the forming the source/drain of the cell transistor.

15. The method of claim 9, wherein a power line is additionally formed for supplying a power voltage to the plate node electrode via another contact electrode of the interlayer insulating film during the step of depositing a conductive film on top of the interlayer insulating film and patterning the same.